Kenneth A. House

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Semiconductor Architecture and RTL Design

SUMMARY OF QUALIFICATIONS:

Major contributor on many successful microprocessor, semiconductor and computer engineering projects through concept, specification, RTL design, verification, documentation, productization, debug, manufacture and customer support.

Recognized opportunities, devised solutions and worked with the team and management to get buy in. Coordinated across disciplines to develop realistic architecture and goals, then delivered quality RTL to meet function, performance, power and schedule goals. Some examples:

- Invented efuse reprogramming logic to improve silicon debug and manufacturing yield.
- Redesigned cache redundancy efuse coding to increase the available number of row/column replacements by as much as a factor of two, providing a significant improvement in yield.
- Invented SCSI bus extender logic to enable a workstation design to be ported to a low-end server, allowing reuse of our ASIC which saved money and brought the schedule in for both systems.

Hardware expertise in microarchitecture, RTL design and debug, chip-pervasive logic, DFT, system design and debug, verification, trouble-shooting. Current design languages include Verilog, VPERL; previous use of Altera MAX+PLUS II, DECSIM, M4, PALASM. Nine hardware patents.

Software experience includes scripting, utilities, modeling, drivers, diagnostics, firmware, process control, applications. Current software languages include Perl, UNIX shell scripting, Python, C; previous use of assembler (x86, VAX, PDP-11, PDP-8, 68000, TI 960a), DCL, FORTRAN, BASIC.

I have worked as an individual contributor and team leader, across disciplines and with global teams.

EXPERIENCE:

K. A. House Consulting; MA 2011-present
Consulting and contract services in hardware and software engineering

Microprocessor/ASIC/FPGA/system design, RTL, DFT, RAS, power management, I/O, firmware, diagnostics, drivers, software, debug.

- Advanced Micro Devices (2012-present) - Microarchitecture and RTL design for the AMD Opteron A1100, responsible for SoC integration of DDR and SATA IP. Front-end CDC and linting design checks.
- Teradyne (2012) – RTL design for a tester FGPA, behavioral modeling.

EXPERIENCE (continued):

Advanced Micro Devices (AMD); Boxborough MA 2004-2011
Senior Member of the Technical Staff

Microprocessor design - Owned microarchitecture and RTL for efuse controller, secure re-fusing logic, thermal monitor/controller and JTAG, chip-pervasive logic, internal and external interfaces, DFT/DFM. Participated in SOC RTL, IP integration, top-level design checks for CDC (0in) and linting (Leda), logic verification, documentation. Contributed to production support. Owned RTL for a test chip.

Miscellaneous - Managed RTL team developing the physical design of a memory interface and an external buffer chip. Consultant for other design teams on issues related to thermal and fuse logic. Member of Emergency Response team, Community Affairs Committee, led Employees Matter Committee.

Sun Microsystems, Inc.; Burlington MA 1999-2004
Senior Staff Engineer - Hardware

Architect, RTL lead and manager for several blocks of the UltraSparc V CPU, including power-on, reset, clock control, power management, DFT, RAS, manufacturing test, selftest, debug, efuse control, thermal monitoring and control, internal interfaces. Many of these features improved testability, reduced debug time and contributed to higher yields. Led a team of microarchitects and RTL designers. Worked with system partners, fab vendor and internal productization teams to improve test and debug features.

Digital Equipment Corporation / Compaq; Maynard MA 1982-1999
Principal Hardware Engineer

Computer architect, hardware and software design engineer, firmware and diagnostics developer for Alpha, MicroVAX and PDP-8 workstations.

Led Alpha workstation development team; verification team leader for core logic ASIC and system printed-circuit boards; debugged Verilog code, board schematics, firmware, drivers, prototype and production hardware; designed CPLD glue logic to work around bugs in third-party components; worked with component vendors to isolate and fix problems, and to improve performance and reliability of hardware and drivers; wrote system specs and trained field service personnel; member of corporate standards committees on Alpha Architecture, Terminal Interface Architecture, SCSI; our product team was recognized for exceeding aggressive cost and schedule goals.

K. A. House Consulting; CA, NH, MA 1977-1992
Consulting and contract services in hardware and software engineering, clinical research

ASIC/FPGA/system design, RTL, DFT, RAS, power management, I/O, firmware, software, debug, biomechanics, EMG signal processing.

Clients included Digital Equipment Corporation, Polaroid, Ruben Engineering, Beckman Instruments, General Electric, Shriners' Hospital (San Francisco), Children’s Hospital (Boston), Rancho Los Amigos Hospital.

EDUCATION:

- Massachusetts Institute of Technology; Cambridge MA
- Bachelor's Degree in Mechanical Engineering

HONORS, PATENTS, PUBLICATIONS:

- AMD Corporate Technical Achievement Award
- AMD President's Award
- Nine patents in I/O, signaling, logic, DFT
- One publication in workstations design

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PATENTS:

Nine patents in I/O, signaling, logic, DFT. Over 140 citations.

U.S Patent 8,402,241: Method and apparatus to control access to device enable features; Miranda, House, Bachand; 2013

U.S. Patent 7,260,759: Method and apparatus for an efficient memory built-in self test architecture for high performance microprocessors; Zarrineh, House, Obaidulla; 2007

U.S. Patent 7,228,474: Semiconductor device and method and apparatus for testing such a device; Williams, House, Siegel; 2007

U.S. Patent 7,206,979: Method and apparatus for at-speed diagnostics of embedded memories; Zarrineh, House, Kim; 2007

U.S. Patent 6,996,491: Method and system for monitoring and profiling an integrated circuit die temperature; Gold, Gauthier, House, Siegel; 2006

U.S. Patent 6,937,958: Controller for monitoring temperature; Gold, Gauthier, House, Zarrineh; 2005

U.S. Patent 6,774,653: Two-pin thermal sensor calibration interface; Gold, House, Gauthier; 2004

U.S. Patent 6,700,946: System and Method for Automatic Generation of an At-Speed Counter; Zarrineh, House, Siegel; 2004

U.S. Patent 5,274,783: SCSI Interface Employing Bus Extender and Auxiliary Bus; House, Kirk, Narhi; 1993

PUBLICATIONS:

DIGITAL Personal Workstations: The Design of High-performance, Low-cost Alpha Systems; Weiss, House; Digital Technical Journal; 1997